CLAIMS

By this response, no claims are amended, added, or canceled. For the Examiner's convenience, a copy of all pending claims and a status of the claims are provided below.

1-13 (canceled)

14. (original) A circuit, comprising:

a lower semiconductor device having an active region comprising a semiconductor with a first crystal orientation; and

an upper semiconductor device having an active region comprising a semiconductor with a second crystal orientation, wherein the upper semiconductor device is formed separately from the lower semiconductor device and connected thereto by an interconnect structure.

15. (original) The circuit of claim 14, wherein the first crystal orientation is different from the second crystal orientation.

16. (original) The circuit of claim 14, further comprising at least one layer of a semiconductor device between the lower and upper semiconductor devices.

17. (original) The circuit of claim 16, wherein at least one semiconductor device of the at least one layer of semiconductor device comprises an active region

having a crystal orientation different from the crystal orientation of at least any one of the lower semiconductor device and the upper semiconductor device.

18. (original) The circuit of claim 14, wherein the upper semiconductor device is bonded to the top of the lower semiconductor device with an insulating layer, and wherein at least a portion of the upper semiconductor device is electrically connected to at least a portion of the lower semiconductor device.

19. (original) The circuit of claim 18, wherein:

the lower semiconductor device includes either a pFET device or an nFET device, and the upper semiconductor device includes either a pFET device or an nFET device; and

the crystal orientation of the active region of the respective lower semiconductor device is different from the crystal orientation of the active region of the respective upper semiconductor device.

20. (original) The circuit of claim 18, wherein the lower and upper semiconductor devices comprise an inverter, and the pFET device has a crystal orientation of [100] in an active region and the nFET device has a crystal orientation of [110] in an active region.

21. (previously presented) The circuit of claim 18, further comprising a gate oxide formed on a top of the active region of the upper semiconductor device.

22. (previously presented) The circuit of claim 21, further comprising a poly gate formed on top of the gate oxide, with an upper poly contact to voltage bus.

23. (previously presented) The circuit of claim 22, further comprising metal contacts connecting to inputs of the upper semiconductor device.

24. (previously presented) The circuit of claim 23, further comprising a lower poly contact connecting to the voltage bus.